Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A transparent latch circuit comprising:
a first latch circuit for receiving a data signal and latching the data signal in response to a first signal fluctuating periodically;
a second latch circuit for receiving an output signal of said first latch circuit and latching the output signal of said first latch circuit in response to a second signal complementary to the first signal; and
latch stop means for receiving an externally input test signal and causing one of said first and second latch circuits to have the signal received by the latch circuit pass therethrough when the test signal is in an inactive state.

[c2] 2. The transparent latch circuit of claim 1,
wherein said latch stop means comprises:
a logic gate for receiving the first signal and the test signal, and outputting the second signal when the test signal is in the active state, or for outputting a latch stop signal when the test signal is in the inactive state; and
said second latch circuit permits the signal output by the first latch circuit to pass through during a period
wherein said second latch circuit receives a latch stop

signal.

[c3] 3. The transparent latch circuit of claim 1, wherein said latch stop means comprises:
a logic gate for receiving the second signal and the test signal, and outputting the first signal when the test signal is in the active state or outputting a latch stop signal when the test signal is in the inactive state; and
said first latch circuit permits a data signal to pass through during a period wherein said first latch circuit receives the latch stop signal.

[c4] 4. The transparent latch circuit of claim 1, wherein said latch stop means comprises:
a plurality of first latch stop means for permitting a signal received by the first latch circuit to pass through when the test signal is in the inactive state;
a plurality of second stop means for permitting a signal received by said second latch circuit to pass through when the test signal is in the inactive state;
wherein said transparent latch circuit is comprised of a first transparent latch circuit including said first latch stop means and a second transparent latch circuit including second latch stop means; and
said first and second transparent latch circuits are alternately interconnected.